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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,988	04/02/2001	William A. Hughes	5500-66500	1347

7590 04/13/2005

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,988	HUGHES ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004 and 10 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49 and 63-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *50-62* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09 September 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-49 and new claims 50-71 have been considered. Claims 3, 6, 26, 35, and 38 have been amended as per Applicant's request. New claims 50-71 have been added as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 09 September 2004; IDS as filed 09 September 2004; and Amendment as received on 10 January 2005.

Allowable Subject Matter

3. Claims 50-62 allowed. Claims 50-62 contain allowable subject matter. The independent claims 60 and 63 include the limitations

a. Wherein the circuit is configured to generate a mode indication responsive to the enable indication and the paging indication

b. Wherein the mode indication is indicative of whether or not a first mode of the processor is active

c. The first mode permitting an address size greater than 32 bits and an operand size greater than 32 bits.

4. The Prior Art of record nor the prior art searched teaches, in essence, that whether the address and operand sizes are greater than 32 bits are dependent on an enable and paging indications.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 11-24, 31-36, 43-49, and 66 are rejected under 35 U.S.C. 102(b) as being taught by James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley).

7. Referring to claim 1, Turley has taught an apparatus comprising:

a. A first storage location configured to store a first indication, the first storage location addressable by a first instruction defined by a processor architecture (Turley page 2; page 7; page 10; page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

b. A second storage location configured to store a second indication, the second storage location addressable by a second instruction defined by the processor architecture, the second instruction being different from the first instruction (Turley page 2; page 7; page 10; page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

c. A third storage location configured to store a mode indication, the mode indication indicative of whether or not a first mode defined in the processor architecture is active (Turley page 2; page 7; page 10; page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57); and

d. A processor configured to generate the mode indication responsive to the first indication and the second indication (Turley pages 53-54).

8. Referring to claims 2, 22, 34, Turley has taught wherein the first indication is an enable indication defined in the processor architecture to indicate whether or not the first mode is to be enabled (Turley page 26, Control Registers and page 28).

9. Referring to claims 3, 23, 35, Turley has taught wherein the second indication is a paging indication defined in the processor architecture to indicate of whether or not paging is enabled (Turley page 26, Control Registers and page 28).

10. Referring to claims 4, 24, 36, Turley has taught wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled (Turley page 26, Control Registers and page 28).

11. Referring to claims 11, 31, 43, Turley has taught a fourth storage location configured to store a segment selector identifying a segment descriptor including a first operating mode indication and a second operating mode indication (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57), and wherein the processor is configured to generate an operating mode responsive to the mode indication, the first operating mode indication, and the second operating mode indication (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

12. Referring to claim 12, Turley has taught wherein the first storage location is located within a first register defined by the processor architecture, and wherein the second storage location is located within a second register defined by the processor architecture (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

13. Referring to claims 13 and 32, Turley has taught wherein the third storage location is located within the first register (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

14. Referring to claim 14, Turley has taught wherein the first register and the second register are incorporated within the processor (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

15. Referring to claim 15, Turley has taught a circuit coupled to the first register and the second register, wherein the circuit is configured to generate the mode indication for storage in the third storage location (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

16. Referring to claim 16, Turley has taught wherein the processor implements the processor architecture (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

17. Referring to claim 17, Turley has taught wherein the processor emulates the processor architecture (Turley pages 27 and 259-260).

18. Referring to claim 18, Turley has taught wherein the processor executes interpreter software for interpreting instructions defined in the processor architecture (Turley page 27 and 259-260).

19. Referring to claim 19, Turley has taught wherein the processor executes translator software for translating instructions defined in the processor architecture to instructions executable by the processor (Turley page 27 and 259-260).

20. Referring to claim 20, Turley has taught wherein the processor executes a combination of: (i) interpreter software for interpreting instructions defined in the processor architecture (Turley page 27 and 259-260); and (ii) translator software for translating instructions defined in the processor architecture to instructions executable by the processor (Turley page 27 and 259-260).

21. Referring to claim 21, Turley has taught a processor comprising:

a. A first register configured to store a first indication, the first register addressable by a first instruction (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

b. A second register configured to store a second indication, the second register addressable by a second instruction different from the first instruction (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57); and

c. A circuit coupled to the first register and the second register, wherein the circuit is configured to generate a mode indication responsive to the first indication and the second indication (Turley pages 53-54),

d. Wherein the mode indication is indicative of whether or not a first mode defined in a processor architecture of the processor is active (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57), and

e. Wherein the circuit is configured to store the mode indication in a location addressable by an instruction (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

22. Referring to claim 33, Turley has taught a method comprising:

a. Storing a first indication in a first storage location addressable by a first instruction (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

b. Storing a second indication in a second storage location addressable by a second instruction (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

c. Generating a mode indication indicative of whether or not a first mode defined in a processor architecture is active (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57), the generating responsive to the first indication and the second indication (Turley pages 53-54); and

d. Storing the mode indication in a third addressable storage location (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

23. Referring to claim 44, Turley has taught a carrier medium carrying a set of instructions for activating a first mode in a processor, the set of instructions including:

a. A first one or more instructions to update a first indication to indicate that physical address extension is enabled (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

b. A second one or more instructions to update a page table base register to point to a set of page tables (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

c. A third one or more instructions to update an enable indication to an enabled state (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57); and

d. A fourth one or more instructions to update a paging indication to indicate that paging is enabled (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

24. Referring to claim 45, Turley has taught wherein an order of the first one or more instructions, the second one or more instructions, and the third one or more instructions in the set of instructions is arbitrary (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

25. Referring to claim 46, Turley has taught wherein the fourth one or more instructions are ordered subsequent to the first one or more instructions, the second one or more instructions, and the third one or more instructions in the set of instructions (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

26. Referring to claim 47, Turley has taught wherein the set of instructions further includes a fifth one or more instructions to update the paging indication to indicate that paging is disabled,

the fifth one or more instructions ordered prior to the first one or more instructions, the second one or more instructions, the third one or more instructions, and the fourth one or more instructions in the set of instructions (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

27. Referring to claim 48, Turley has taught a carrier medium carrying a set of instructions for deactivating a first mode in a processor, the set of instructions including:

a. A first one or more instructions to update a paging indication to indicate that paging is disabled (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

b. A second one or more instructions to update a page table base register to point to a set of page tables (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57); and

c. A third one or more instructions to update an enable indication to a disabled state (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

28. Referring to claim 49, Turley has taught wherein the set of instructions further includes a fourth one or more instructions to update the paging indication to indicate that paging is enabled (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

29. Referring to claim 66, Turley has taught a computer readable medium storing a plurality of instructions which, when executed:

a. Responsive to a first instruction, update a first storage location configured to store a first indication (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

b. Responsive to a second instruction, update a second storage location configured to store a second indication (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57);

c. Generate a mode indication responsive to the first indication and the second indication (Turley pages 53-54), the mode indication indicative of whether or not a first mode is active in a processor (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57); and

d. Update a third storage location configured to store the mode indication (Turley page 26, Control Registers; page 28; page 49, Table A segment descriptor; pages 50-54; and page 57).

30. Referring to claim 69, Turley has taught wherein the first indication is an enable indication indicative of whether or not the first mode is to be enabled (Turley page 26, Control Registers and page 28).

31. Referring to claim 70, Turley has taught wherein the second indication is a paging indication indicative of whether or not paging is enabled (Turley page 26, Control Registers and page 28).

32. Referring to claim 71, Turley has taught wherein the mode indication indicates that the first mode is active if the enable indication is in an enabled state and the paging indication indicates that paging is enabled (Turley page 26, Control Registers and page 28).

Claim Rejections - 35 USC § 103

33. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

34. Claims 5-10, 25-30, and 37-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley), as applied to claims 3, 23, and 24 above, in view of Van Dyke et al., U.S. Patent Number 6,418,524 (herein referred to as Van Dyke).

35. Referring to claims 5-10 and 25-30, Turley has taught

a. Wherein the processor is configured to check a status of one or more indications including the enable indication when changing one of the one or more indications to ensure that the change is permitted by the processor architecture (Applicant's claims 5 and 25) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178); and

b. Wherein the processor is configured to signal an exception prior to changing the one of the one or more indications if the change is not permitted (Applicant's claims 6 and 26) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

36. Turley has not taught

a. Wherein the processor is configured to check a status of one or more indications including the paging indication (Applicant's claims 5 and 25);

b. Wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claims 7 and 27);

c. Wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claims 8 and 28);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled (Applicant's claims 9 and 29); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claims 10 and 30).

37. Van Dyke has taught

a. Wherein the processor is configured to check a status of one or more indications including the paging indication (Applicant's claims 5 and 25) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

b. Wherein, if the enable indication is changed from a disabled state to an enabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claims 7 and 27) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

c. Wherein, if the enable indication is changed from an enabled state to a disabled state, the processor checks that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claims 8 and 28) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that physical address extension is disabled (Applicant's claims 9 and 29) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claims 10 and 30) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2).

38. In regards to Van Dyke, teaching that segmentation and paging are dependent means that one must indicate the correct mode in order for the other to be enabled. A person of ordinary skill in the art at the time the invention was made, and as taught by Van Dyke, would have recognized that having segmentation and paging dependent allows compatibility and use in newer and/or more advance microprocessor architectures (Van Dyke column 1, lines 60-64), thereby increasing compatibility and usability. Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to incorporate the segmentation and paging dependency to increase compatibility and usability.

39. Referring to claims 37-42, Turley has taught

a. Checking a status of one or more indications including the enable indication and when changing one of the one or more indications to ensure that the change is permitted by the processor architecture (Applicant's claim 37) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

b. Signaling an exception prior to changing the one of the one or more indications if the change is not permitted (Applicant's claim 38) (Turley pages 18-34, 47-54, 79-81, 142-145, and 178).

40. Turley has not taught

a. Checking a status of one or more indications including the enable indication and the paging indication (Applicant's claim 37);

b. Wherein the checking comprises, if the enable indication is changed from a disabled state to an enabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 39);

c. Wherein the checking comprises, if the enable indication is changed from an enabled state to a disabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 40);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the

enable indication is in an enabled state and another indication indicates that physical address extension is disabled (Applicant's claim 41); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claim 42).

41. Van Dyke has taught

a. Checking a status of one or more indications including the enable indication and the paging indication (Applicant's claim 37) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

b. Wherein the checking comprises, if the enable indication is changed from a disabled state to an enabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 39) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

c. Wherein the checking comprises, if the enable indication is changed from an enabled state to a disabled state, checking that the paging indication indicates that paging is disabled for the change to be permitted (Applicant's claim 40) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2);

d. Wherein, if the paging indication is changed from indicating that paging is disabled to indicating that paging is enabled, the change is not permitted if the enable indication is in an enabled state and another indication indicates that

physical address extension is disabled (Applicant's claim 41) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2); and

e. Wherein the one of the one or more indications is an indication of whether or not physical address extension is enabled, and wherein the change is not permitted if the enable indication is in an enabled state (Applicant's claim 42) (Van Dyke column 1, lines 23-25 and 41-64; column 2, lines 14-54; Figure 1; and Figure 2).

42. In regards to Van Dyke, teaching that segmentation and paging are dependent means that one must indicate the correct mode in order for the other to be enabled. A person of ordinary skill in the art at the time the invention was made, and as taught by Van Dyke, would have recognized that having segmentation and paging dependent allows compatibility and use in newer and/or more advance microprocessor architectures (Van Dyke column 1, lines 60-64), thereby increasing compatibility and usability. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the segmentation and paging dependency to increase compatibility and usability.

43. Claims 63-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley) in view of The American Heritage® Dictionary of the English Language Fourth Edition ©2000 (herein referred to as (herein referred to as American Heritage).

44. Referring to claims 63-65, Turley has taught a computer system comprising the processor as recited in claim 21. Please see the rejection of claim 21 above for more details on these limitations. Turley has not taught a device configured to communicate between the computer system and another computer system (Applicant's claim 63), a network interface circuit

(Applicant's claim 64), and a modem (Applicant's claim 65). American Heritage has taught a computer network (American Heritage "network") and modem (American Heritage "modem). In regards to American Heritage, the network interface circuit is inherent to the computer network. In order to be able to translate the data into understandable signals for the modem and/or network to transmit, the network interface circuit is needed to perform this translation. A person of ordinary skill in the art at the time the invention was made, and as taught by American Heritage, a computer network shares information between computers (American Heritage "network"), thereby allowing data to be used by a plurality of users at different computer stations. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the network and modem of American Heritage in the device of Turley to allow data to be used by other users at different computers.

45. Claims 67-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over James L. Turley's Advanced 80836 Programming Techniques (herein referred to as Turley), as applied to claim 66 above, in view of The American Heritage® Dictionary of the English Language Fourth Edition ©2000 (herein referred to as (herein referred to as American Heritage). Turley has not taught

a. Wherein the plurality of instructions emulate the first instruction and the second instruction (Applicant's claim 67);

b. Wherein the plurality of instructions are executed in place of the first instruction and the second instruction (Applicant's claim 68).

46. American Heritage has taught

a. Wherein the plurality of instructions emulate the first instruction and the second instruction (Applicant's claim 67) (American Heritage "emulate");

b. Wherein the plurality of instructions are executed in place of the first instruction and the second instruction (Applicant's claim 68) (American Heritage "emulate").

47. In regards to American Heritage, the modification to software means software instructions. A person of ordinary skill in the art at the time invention was made, and as taught by American Heritage, would have recognized that the emulation instructions allow a system to accept the same data, execute the same programs, and achieve the same results as another system (American Heritage "emulate"), thereby increasing compatibility of the current system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the emulator of American Heritage in the device of Turley to increase compatibility.

Response to Arguments

48. Applicant's arguments filed 09 September 2005 have been fully considered but they are not persuasive. Applicant argues in essence on pages 14-19

> Applicants respectfully submit that the portion of Turley cited in the present Office Action is not designated as nearly as practicable and the alleged pertinence of Turley is not clearly explained.
>
> ...**Applicants respectfully request that either the Examiner withdraw the rejection or specifically point out the teachings of Turley that are alleged to correspond to each of the claim features** with the specificity required by the above highlighted rules...

49. This has not been found persuasive. The Examiner has narrowed the scope of the citations above, as requested. However, the Examiner does not feel the Applicant's statement that is was "not designated as nearly as practicable and the alleged pertinence of Turley is not clearly explained" is appropriate. Turley is a textbook that covers almost the entirety of Intel's 80386 processor architecture in a total of 509 pages. The Examiner in the previous Office Action merely cited 33 pages, which is 6.48% of the entire book. All sections cited were deemed necessary to understand the elements and their functions, since these 33 pages adequately described how these limitations functioned similarly to the claimed subject matter. To further the understanding, the Examiner has included the tables below to further clarify the mappings of the claims to the references.

50. Claim 1's limitations and their mappings to the prior art reference are shown below.

Applicant's limitation	Prior Art Reference
An apparatus comprising	
A first storage location configured to store a first indication,	Turley Page 26, Control Registers describes and shows the format of the Control registers which store indication bits and values. Page 28 has more details on the control registers. Page 49, Table A segment descriptor describes the segment descriptor, which also stores indications, Pages 50-54 describe and show the individual indicators in the

	segment descriptor. Page 57 describes one of the indicators in the segment descriptor in more detail.
The first storage location addressable by a first instruction defined by a processor architecture	Turley Page 2, paragraph 3 Page 7 Page 10, Instruction Set All of these pages describe how the 80386 instruction set allows developers to control the operation of the memory segmentation, i.e. controlling the values of the bits, and control registers.
A second storage location configured to store a second indication,	Turley Page 26, Control Registers describes and shows the format of the Control registers which store indication bits and values. Page 28 has more details on the control registers. Page 49, Table A segment descriptor describes the segment descriptor, which also stores indications, Pages 50-54 describe and show the individual indicators in the segment descriptor. Page 57 describes one of the indicators in the segment descriptor in more detail.
The second storage location	Turley Page 2, paragraph 3

addressable by a second instruction defined by the processor architecture, the second instruction being different from the first instruction	Page 7 Page 10, Instruction Set All of these pages describe how the 80386 instruction set allows developers to control the operation of the memory segmentation, i.e. controlling the values of the bits, and control registers.
A third storage location configured to store a mode indication,	Turley Page 26, Control Registers describes and shows the format of the Control registers which store indication bits and values. Page 28 has more details on the control registers. Page 49, Table A segment descriptor describes the segment descriptor, which also stores indications, Pages 50-54 describe and show the individual indicators in the segment descriptor. Page 57 describes one of the indicators in the segment descriptor in more detail. The modes are the resultant operating modes from whether the

	indication bits are set or not. For example, the Default size bit described on page 52 sets a 16 bit size operating more or a 32 bit size operating mode.
The mode indication indicative of whether or not a first mode defined in the processor architecture is active	Turley Page 26, Control Registers describes and shows the format of the Control registers which store indication bits and values. Page 28 has more details on the control registers. Page 49, Table A segment descriptor describes the segment descriptor, which also stores indications, Pages 50-54 describe and show the individual indicators in the segment descriptor. Page 57 describes one of the indicators in the segment descriptor in more detail. The modes are the resultant operating modes from whether the indication bits are set or not. For example, the Default size bit described on page 52 sets a 16 bit size operating more or a 32 bit size operating mode.
A processor configured to generate the mode indication responsive to the	Turley pages 53-54 Applicant does not provide details in this claim on how the enable indication, first operating mode indication, and second operating mode indication interact to establish a default address size. Applicant has only claimed that these three indications are used in some

first indication and the second indication	undefined way to establish the default address size. The signals indicated above interact in the following manner to establish a default address size. First, the PE bit in Control Register 0 must be set to enable protected mode (Turley page 26, Control Register 0, PE) in order for segmentation to even be possible (Turley page 45, paragraph 2 "...the method of segmentation used in Protected mode" and page 47, paragraph 2 "...concept of a segment...running in Protected mode"). In essence, when the PE bit is not set, the segmentation described is disabled and, when the PE bit is set, the segmentation is enabled. Second, the DPL bit must match to allow access to the segment of memory. If access is not granted to the segment of memory, the segment cannot be accessed to set the address size. Finally, the G bit establishes the address size, since it is used as the default for determining the address size represented by the Limit field. The G bit indicates whether the address space size spans one megabyte (1MB) of space or up to four gigabytes (4GB) of space. Therefore, in order to establish a default address size, Protected mode must be enabled by the PE bit, the DPL bit must indicate that segment memory is accessible, and the G bit is accessed to establish the address size.

51. Claim 1's limitations and their equivalent limitations in claim 21. Therefore, the art which read upon the limitation in the above table will read on the corresponding limitation in

claim 21. Claim 63 incorporates some of the limitations of claim 21, so the rejections applicable to these limitations of claim 21 are applicable to the matching limitations in claim 63.

Claim 1 Limitation	Claim 21 Limitation
An apparatus comprising	A processor comprising:
A first storage location configured to store a first indication,	A first register configured to store a first indication,
The first storage location addressable by a first instruction defined by a processor architecture	The first register addressable by a first instruction
A second storage location configured to store a second	A second storage location configured to store a second indication,

indication,	
The second storage location addressable by a second instruction defined by the processor architecture, the second instruction being different from the first instruction	The second register addressable by a second instruction different from the first instruction; and
A third storage location configured to store a mode indication,	Wherein the circuit is configured to store the mode indication in a location addressable by an instruction
The mode indication indicative of	Wherein the mode indication is indicative of whether or not a first mode defined in the processor architecture of the processor is active

whether or not a first mode defined in the processor architecture is active	
A processor configured to generate the mode indication responsive to the first indication and the second indication	A circuit coupled to the first register and the second register, where in the circuit is configured to generate a mode indication responsive to the first and second indication,

52. Claim 1's limitations and their equivalent limitations in claim 33. Therefore, the art which read upon the limitation in the above table will read on the corresponding limitation in claim 33.

Claim 1 Limitation	Claim 33 Limitation
An apparatus comprising	A method comprising:

A first storage location configured to store a first indication,	Storing a first indication in a first storage location
The first storage location addressable by a first instruction defined by a processor architecture	The first storage location addressable by a first instruction
A second storage location configured to store a second indication,	Storing a second indication in a second storage location
The second storage location addressable by a second instruction	The second storage location addressable by a second instruction

defined by the processor architecture, the second instruction being different from the first instruction	
A third storage location configured to store a mode indication,	Storing the mode indication in a third addressable storage location
The mode indication indicative of whether or not a first mode defined in the processor architecture is active	Generating a mode indication indicative of whether or not a first mode defined in a processor architecture is active

A processor configured to generate the mode indication responsive to the first indication and the second indication	The generating responsive to the first indication and the second indication

53. Claim 44's limitations and their mappings to the prior art reference are shown below.

Applicant's limitation	Prior Art Reference
A carrier medium carrying a set of instructions for activating a first mode in a processor, the set of instructions including:	
To update a first	Turley

indication to indicate that physical address extension is enabled	Page 49, Table A segment descriptor describes the segment descriptor, which also stores indications, Pages 50-54 describe and show the individual indicators in the segment descriptor. Page 57 describes one of the indicators in the segment descriptor in more detail. When the D bit is set, the maximum stack size is 4GB, but when it is not set the maximum stack size is 64KB. The Granularity bit allows for the address in the segment descriptor size to be increased.
A first one or more instructions	Turley Page 2, paragraph 3 Page 7 Page 10, Instruction Set All of these pages describe how the 80386 instruction set allows developers to control the operation of the memory segmentation, i.e. controlling the values of the bits, and control registers.
To update a page table base register to point to a set of page tables	Turley Page 28, Control Register 3
A second one or	Turley

more instructions	Page 2, paragraph 3 Page 7 Page 10, Instruction Set All of these pages describe how the 80386 instruction set allows developers to control the operation of the memory segmentation, i.e. controlling the values of the bits, and control registers.
To update an enable indication to an enabled state	Turley Page 26, Control Registers describes and shows the format of the Control registers which store indication bits and values. Page 28 has more details on the control registers. Page 49, Table A segment descriptor describes the segment descriptor, which also stores indications, Pages 50-54 describe and show the individual indicators in the segment descriptor. Page 57 describes one of the indicators in the segment descriptor in more detail. The modes are the resultant operating modes from whether the indication bits are set or not. For example, the Default size bit described on page 52 sets a 16 bit size operating more or a 32 bit size operating mode.
A third one or more instructions	Turley Page 2, paragraph 3

	Page 7 Page 10, Instruction Set All of these pages describe how the 80386 instruction set allows developers to control the operation of the memory segmentation, i.e. controlling the values of the bits, and control registers.
To update a paging indication to indicate that paging is enabled	Turley Page 27, PG
A fourth one or more instructions	Turley Page 2, paragraph 3 Page 7 Page 10, Instruction Set All of these pages describe how the 80386 instruction set allows developers to control the operation of the memory segmentation, i.e. controlling the values of the bits, and control registers.

54. Claim 44's limitations and their equivalent limitations in claim 48. Therefore, the art which read upon the limitation in the above table will read on the corresponding limitation in claim 48.

Claim 44 Limitation	Claim 48 Limitation

A carrier medium carrying a set of instructions for activating a first mode in a processor, the set of instructions including:	A carrier medium for carrying a set of instructions for deactivating a first mode in a processor, the set of instructions including:
A first one or more instructions to update a first indication to indicate that physical address extension is enabled	A first one or more instructions to update a first indication to indicate that physical address extension is enabled
A second one or more instructions to update a page table base register to point	A second one or more instructions to update a page table base register to point to a set of page tables

to a set of page tables	
A third one or more instructions to update an enable indication to an enabled state	A third one or more instructions to update an enable indication to a disabled state In regards to this claim limitation, whether the state is enabled or disabled does not matter. If the state is enabled by the reference, then there is a disabled state for the reference inherently.

55. Claim 1's limitations and their equivalent limitations in claim 66. Therefore, the art which read upon the limitation in the above table will read on the corresponding limitation in claim 66.

Claim 1 Limitation	Claim 66 Limitation
An apparatus comprising	A computer readable medium storing a plurality of instructions which, when executed:
A first storage location configured to store a first indication,	Update a first storage location configured to store a first indication;
The first storage	Responsive to a first instruction,

location addressable by a first instruction defined by a processor architecture	
A second storage location configured to store a second indication,	Update a second storage location configured to store a second indication;
The second storage location addressable by a second instruction defined by the processor architecture, the second instruction being different from	Responsive to a second instruction,

the first instruction	
A third storage location configured to store a mode indication,	Update a third storage location configured to store the mode indication;
The mode indication indicative of whether or not a first mode defined in the processor architecture is active	The mode indication indicative of whether or not a first mode is active in a processor;
A processor configured to generate the mode indication responsive to the first indication	Generate a mode indication responsive to the first indication and the second indication,

and the second indication	

Conclusion

56. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

57. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

58. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

59. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

60. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
31 March 2005

RICHARD L. ELLIS
PRIMARY EXAMINER